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PATENT NUMBER and
ISSUE DATE

10046805
U.S. PRO
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U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10046805	01/14/2002	438	674	2812	2329 Kilday

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(6-5 27-30 → Class 257/734+

→ Claims 1-27 and 31-62
Class 438/674

**CONTINUING DATA VERIFIED:

1AC none 6/26/03

** FOREIGN APPLICATIONS VERIFIED:

1AC none 6/26/03

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	ATTORNEY DOCKET NO
Foreign priority claimed 35 USC 119 conditions met		<input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input checked="" type="checkbox"/> yes <input type="checkbox"/> no	WAIC 6/26/03 5649-968
Verified and Acknowledged Examiner's initials			
TITLE : Methods of forming metal layers in integrated circuit devices using selective deposition on edges of recesses and conductive contacts so formed			

U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims <input type="checkbox"/> Print Claim for O.G.	
		DRAWING Sheets Drwg. <input type="checkbox"/> Figs. Drwg. <input type="checkbox"/> Print Fig. <input type="checkbox"/>	
		Primary Examiner	
ISSUE FEE		Application Examiner	
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